

ESE 2027

Main Examination

UPSC ENGINEERING SERVICES EXAMINATION

Topicwise
**Conventional
Practice Book**

Electrical Engineering

PAPER-II





MADE EASY Publications Pvt. Ltd.

Corporate Office: 44-A/4, Kalu Sarai (Near Hauz Khas Metro Station), New Delhi-110016

E-mail: infomep@madeeasy.in

Contact: 9021300500

Visit us at: www.madeeasypublications.org

ESE Main Examination • Conventional Practice Book : Electrical Engineering PAPER-II

© Copyright, by MADE EASY Publications Pvt. Ltd.

All rights are reserved. No part of this publication may be reproduced, stored in or introduced into a retrieval system, or transmitted in any form or by any means (electronic, mechanical, photo-copying, recording or otherwise), without the prior written permission of the above mentioned publisher of this book.

First Edition: 2023

Reprint: 2024

Reprint: 2025

Reprint: 2026

ESE 2027 Main Examination

Conventional Practice Book

Electrical Engineering

PAPER-II

CONTENTS

Sl. TOPIC	PAGE No.	Sl. TOPIC	PAGE No.
1. Analog Electronics..... 1-39		5. Control Systems..... 122-198	
1. Operational Amplifiers 1		1. Modelling of a Control System and Transfer Function Approach..... 122	
2. Diodes..... 8		2. Block Diagram and Signal Flow Graph 126	
3. Bipolar Junction Transistor..... 17		3. Feedback Systems 134	
4. MOSFET 24		4. Time-Response Analysis..... 140	
5. Multistage and Feedback Amplifiers..... 30		5. Routh-Hurwitz Stability Criterion 151	
2. Digital Electronics..... 40-81		6. Root Locus..... 157	
1. Basics of Digital Circuits 40		7. Frequency Domain Analysis 164	
2. Combinational Circuits..... 46		8. Bode Plot 170	
3. Sequential Circuits 54		9. Polar and Nyquist Plot 176	
4. Memories & Programmable Logical Devices... 60		10. Compensators and Controllers..... 185	
5. Logic Families..... 67		11. State-Space Analysis..... 191	
6. ADCs / DACs 76			
3. Microprocessors 82-101		6. Electrical Machines..... 199-237	
1. 8085 Microprocessor 82		1. Electromechanical Energy Conversion and Magnetic Circuits 199	
2. 8086 Microprocessor..... 96		2. Transformers..... 203	
3. Interfacing & Peripheral Devices..... 99		3. DC Machines..... 210	
4. Communication Systems 102-121		4. Synchronous Machines 216	
1. Analog Modulation..... 102		5. Induction Machine 223	
2. Digital Communication Schemes 107		6. Fractional Kilowatt Machines 234	
3. Information Theory & Error Control Coding... 116		7. Special Machines 236	

7. Power Systems238-317

1. Generating Power Station238
2. Performance of Transmission Line,
Line Parameters and Corona242
3. Compensation Techniques, Voltage-Profile Control
and Load Frequency Control251
4. Distribution System, Cables and Insulator256
5. Fault Analysis.....264
6. Load Flow Studies278
7. Power System Stability284
8. Switchgear and Protection.....293
9. Optimal Power System Operation.....305
10. HVDC Transmission, Facts
and Recent Trends in Power Systems311
11. Power System Transients314

8. Power Electronics318-364

1. Power Semiconductor Devices,
Transistors & Thyristors318

2. Diode Circuits and Rectifiers322
3. Phase Controlled Rectifiers326
4. Choppers336
5. Inverters343
6. Power Semiconductor Drives.....350
7. Resonant Converters358
8. Switched Mode Power Supplies (SMPS)362

9. Systems & Signals Processing.....365-440

1. Basics of Signals and Systems365
2. LTI Systems.....375
3. Fourier Series.....382
4. Fourier Transform390
5. Laplace Transform401
6. Z-transform409
7. DFT + FFT.....419
8. Digital Filter Design430



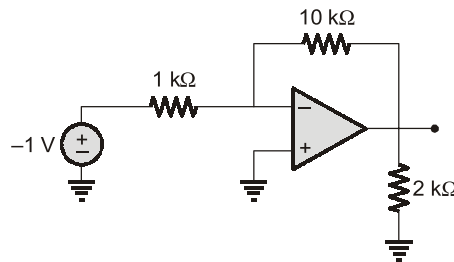
1

Analog Electronics

1. Operational Amplifiers

Level-1

- 1.1 (a) For the circuit shown, find the currents through all branches and the voltages at all nodes.
 (b) Since the current supplied by the OP-AMP is greater than the current drawn from the input signal source, where does the additional current come from. (10 Marks)



Solution:

For an inverting amplifier as we know,

$$\begin{aligned} \frac{V_0}{V_i} &= \frac{-R_2}{R_1} \\ \Rightarrow V_0 &= \frac{-R_2}{R_1} \times V_i \\ V_0 &= \left(\frac{-10}{1} \right) (-1) = 10 \text{ volts} \end{aligned}$$

i_2 can be calculated as

$$i_2 = \frac{V_0}{2K} = 5 \text{ mA}$$

$$\text{also, } i_1 = i_3 = \frac{V_0}{10K} = 1 \text{ mA}$$

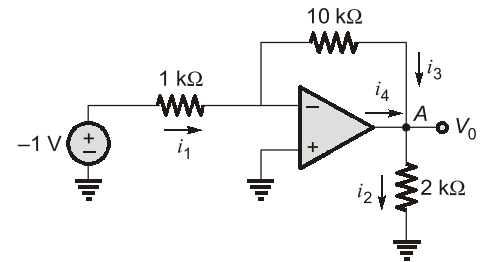
by KCL at point A,

$$i_4 + i_3 = i_2$$

$$\text{Hence, } i_4 = i_2 - i_3$$

$$i_4 = (5 - 1) \text{ mA} = 4 \text{ mA}$$

Hence the additional current comes from the output of the OP-AMP.



- 1.2 An inverting OP-AMP circuit for which the required gain is -50 V/V uses an OP-AMP whose open loop gain is only 200 V/V . If the larger resistor used is $100 \text{ k}\Omega$, to what must the smaller be adjusted? With what resistor must a $2 \text{ k}\Omega$ resistor connected to the input be shunted to achieved this goal?

(Note: A resistor R_a is said is to be shunted by resistor R_b when R_b is placed in parallel with R_a)

(10 Marks)

Solution:

By drawing the figure according to the question

Let the gain of OP-AMP is $A = 200 \text{ V/V}$

$$\therefore V_1 = \frac{-V_0}{A} = \frac{-V_0}{200}$$

and overall close loop gain,

$$\frac{V_0}{V_i} = -50 \text{ V/V}$$

by using KCL at point P .

$$\frac{V_i - \left(\frac{-V_0}{A}\right)}{R_1} = \frac{\left(\frac{-V_0}{A} - V_0\right)}{100K}$$

$$\Rightarrow R_1 = \frac{100K \left[V_i + \frac{V_0}{A} \right]}{- \left[V_0 + \frac{V_0}{A} \right]} = \frac{100K \left[\frac{-V_0}{50} + \frac{V_0}{200} \right]}{- \left[V_0 + \frac{V_0}{200} \right]}$$

$$R_1 = 100K \times \frac{3}{201} = 1.49 \text{ k}\Omega$$

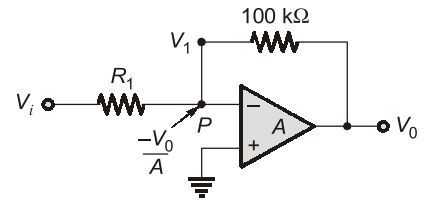
as given in question shunt resistor is R_a ,

$$\text{and } R_a \parallel 2 \text{ k}\Omega = 1.49 \text{ K}$$

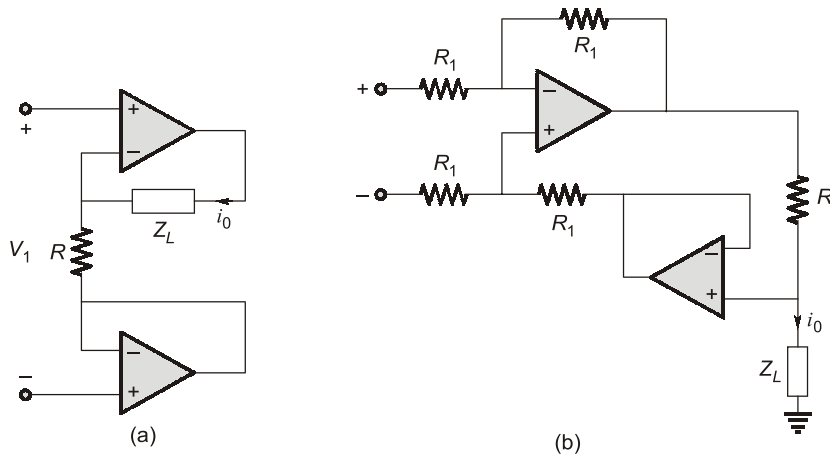
$$\text{So, } \frac{R_a \times 2K}{R_a + 2K} = 1.49 \text{ K}$$

by solving above equation we will get

$$R_a = 5.84 \text{ k}\Omega$$



- 1.3 The two circuits in figures are intended to function as voltage to current converters, that is, they supply the load impedance Z_L with a current proportional to V_1 and independent of the value of Z_L . Show that this is indeed the case, and find for each circuit i_0 as a function of V_1 . Comment on the differences between the two circuits.



(12 Marks)

Solution:

From figure (a):

Since input current for the Op-amp is zero hence V_i appears across the resistance R .

So,
$$i_0 \approx \frac{V_i}{R}$$

From figure (b):

as

$$V_P = Z_L i_0$$

Using superposition,

$$V_I = V_1 - V_2$$

Considering V_1 only

$$V_B = \frac{V_D}{2} = \frac{Z_L i_{01}}{2}$$

KCL at point,

$$\frac{V_1 - \frac{Z_L i_{01}}{2}}{R_1} = \frac{\frac{Z_L i_{01}}{2} - i_{01}(Z_L + R)}{R_1}$$

So,

$$V_1 = i_{01} R \Rightarrow i_{01} = \frac{V_1}{R}$$

Considering $(-V_2)$ only

$$V_B = \frac{-V_2 + Z_L i_{02}}{2}$$

(by super position)

$$V_A = \frac{i_{02} \times (R + Z_L)}{2}$$

as

$$V_A = V_B \text{ hence}$$

$$-V_2 + Z_L i_{02} = i_{02} R + i_{02} Z_L$$

$$-V_2 = i_{02} R$$

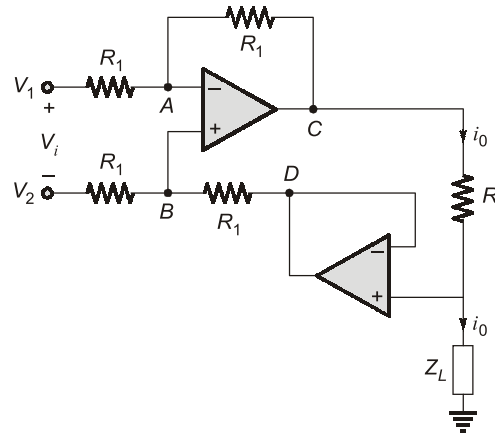
$\Rightarrow$

$$i_{02} = \frac{-V_2}{R}$$

Total current is :

$$i_0 = i_{01} + i_{02} = \frac{V_1}{R} - \frac{V_2}{R} = \frac{V_I}{R}$$

Circuit in figure (a) has infinite input while the circuit (b) has finite input resistance with one side of Z_L is grounded.



1.4 A differentiator utilizes an ideal op-amp, a 10 kΩ resistor and a 0.01 μF capacitor.

- What is the frequency f_0 (in Hz) at which its input and output sine-wave signals have equal magnitude?
- What is the output signals for a 1 volt peak to peak sine wave input with frequency equal to $10f_0$? (10 Marks)

Solution:

(a) We know that for a differentiator

$$\frac{V_0}{V_i}(s) = -SRC = -S \times 0.01 \times 10^{-6} \times 10 \times 10^3 = -10^{-4} S$$

$$\frac{V_o}{V_i}(j\omega) = -j\omega(10^{-4})$$

$$\left| \frac{V_o}{V_i} \right| = -10^{-4} \omega$$

When $\omega = 10^4 \text{ rad/s}$

then $\left| \frac{V_o}{V_i} \right| = 1$

So, $2\pi f = 10^4$

So $f = 1.59 \text{ kHz}$

- (b) When frequency will be 10 times then the output will be 10 times as large as the input 10 volt peak to peak.
 (-j) means the output lags the input by 90°
 So $V_o(t) = -5 \sin(10^5 t + 90^\circ) \text{ Volts}$

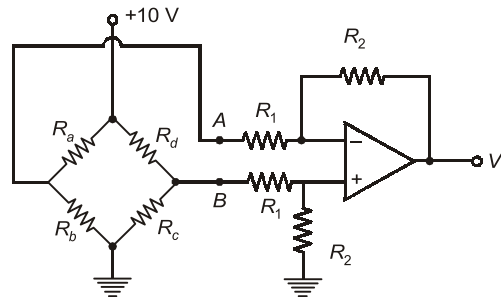
1.5 Consider the circuit shown in figure. The circuit uses an ideal operational amplifier. Assuming that the impedances at nodes A and B do not load the preceding bridge circuit, calculate the output voltage V_o .

(a) when $R_a = R_b = R_c = R_d = 10 \text{ ohms}$.

(b) when $R_a = R_b = R_c = 10 \text{ ohms}$ and $R_d = 120 \text{ ohms}$.

$$R_2 = 12 \text{ k}\Omega$$

$$R_1 = 10 \text{ k}\Omega$$



(5 Marks)

Solution:

(a)
$$V_A = 10 \times \frac{R_b}{R_a + R_b} = 10 \times \frac{100}{100 + 100} = 5 \text{ V}$$

$$V_B = \frac{10 R_C}{R_C + R_D} = 10 \times \frac{100}{100 + 100} = 5 \text{ V}$$

Given op-amp is a differential amplifier

$$\text{So, } V_o = \frac{R_2}{R_1} (V_B - V_A) = \frac{12\text{k}}{10\text{k}} (5 - 5) = 0 \text{ V}$$

(b)
$$V_A = 10 \times \frac{R_b}{R_d + R_b} = 10 \times \frac{100}{100 + 100} = 5 \text{ V}$$

$$V_B = 10 \times \frac{R_c}{R_c + R_d} = 10 \times \frac{100}{100 + 120} = 4.55 \text{ V}$$

$$V_o = \frac{R_2}{R_1} (V_B - V_A) = \frac{12\text{k}}{10\text{k}} (4.55 - 5) = -0.55 \text{ V}$$

Level-2

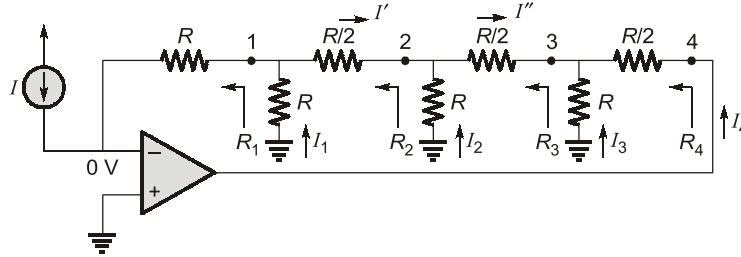
1.6 In the circuit given in the figure,

(a) Find the resistances looking into node 1, R_1 ; node 2, R_2 ; node 3, R_3 ; and node 4, R_4 :

(b) Find the current I_1 , I_2 , I_3 and I_4 in terms of the input current I .

(c) Find the voltages at nodes 1, 2, 3, 4 that is V_1 , V_2 , V_3 and V_4 in terms of (IR)

(15 Marks)



Solution:

(a) From the figure:

$$R_1 = R$$

R_2 can be calculated as:

$$R_2 = (R \parallel R) + \frac{R}{2} = R$$

$$R_3 = (R_2 \parallel R) + \frac{R}{2} = R$$

$$R_4 = (R_3 \parallel R) + \frac{R}{2} = (R \parallel R) + \frac{R}{2} = R$$

(b) As,

$$V = IR$$

So,

$$V_1 = I_1 R$$

and

$$I_1 = I$$

$$I' = I + I = 2I$$

By KVL at node-1

$$V_1 + 2I \left(\frac{R}{2} \right) = RI_2$$

$$I_R + I_R = RI_2$$

So,

$$I_2 = 2I$$

$$I'' = I_2 + I' = 4I$$

By KVL at node-2

$$V_2 + 4I \times \frac{R}{2} = RI_3$$

$$R \times 2I + 4I \times \frac{R}{2} = RI_3$$

hence,

$$I_3 = 4I$$

and

$$I_4 = -[4I + 4I] = -8I$$

(c)

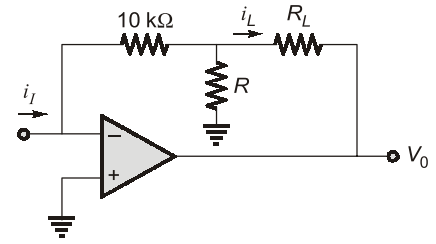
$$V_1 = -I_1 R = -IR$$

$$V_2 = -I_2 R = -2IR$$

$$V_3 = -I_3 R = -4IR$$

$$V_4 = -I_4 R + I_4 \frac{R}{2} = -4IR - \frac{8IR}{2} = -8IR$$

- 1.7 Assuming the Op-amp to be ideal, it is required to design the circuit shown in figure, to implement a current amplifier with gain $i_L/i_I = 20$ A/A



- Find the required value of R .
- If $R_L = 1 \text{ k}\Omega$ and the op-amp operates in an ideal manner so long as V_O is in the range $\pm 12 \text{ V}$. What range of i_I is possible?
- What is the input resistance of the current amplifier? If the amplifier is fed with a current source having a current of 1 mA and a source resistance of $10 \text{ k}\Omega$ find i_L .

(15 Marks)

Solution:

- (a) Given that:

$$\frac{i_L}{i_I} = 20$$

 $\Rightarrow$

$$i_L = 20i_I$$

by KVL :

$$-10 \text{ k}\Omega \times i_I = R(i_I - i_L)$$

$$R = \frac{10 \text{ K} \times i_I}{20i_I - i_I} = 0.53 \text{ k}\Omega$$

- (b) Given $R_L = 1 \text{ k}\Omega$ and range of V_O is $-12 \leq V_O \leq 12 \text{ V}$

by KVL:

$$V_O = R_L i_L + (10 \text{ K}) i_I$$

$$= i_I \left[R_L \frac{i_L}{i_I} + 10 \text{ K} \right]$$

$$V_O = i_I [1 \text{ k} \times 20 + 10 \text{ k}]$$

$$V_O = (30 i_I) \text{ K}$$

$$i_I = \frac{V_O}{30}$$

So,

$$\frac{-12}{30} \leq i_I \leq \frac{12}{30}$$

 $\Rightarrow$

$$-0.4 \text{ mA} \leq i_I \leq 0.4 \text{ mA}$$

- (c) Input resistance of given current amplifier

$$R_I = \frac{V_I}{i_I} = \frac{0}{i_I} = 0$$

as by diagram,

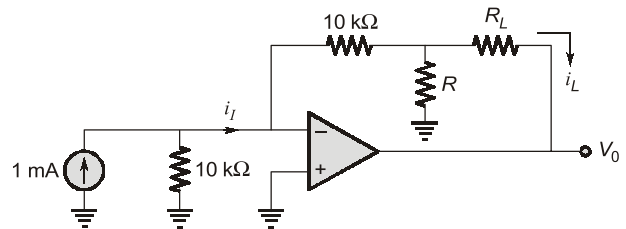
$$i_I = 1 \text{ mA}$$

and

$$i_L = 20 i_I$$

So,

$$i_L = 20 \text{ mA}$$



- 1.8 A designer wanting to achieve a stable gain of 100 V/V at 5 MHz , considers her choice of amplifier topologies. What unity-gain frequency would a single operational amplifier require to satisfy her need? Unfortunately, the best available amplifier has an f_T of 40 MHz .

- How many such amplifiers connected in a cascade of identical non inverting stages would she need to achieve her goal?
- What is the 3-dB frequency of each step she can use?
- What is the overall 3-dB frequency?

(15 Marks)

Solution:

As we know that, $f_T = 100 \times 5 = 500 \text{ MHz}$

If we use single Op-amp

But given in question that best Op-amp has $f_T = 40 \text{ MHz}$, so the possible closed loop gain at 5 MHz is

$$(A) = \frac{40}{5} = 8 \text{ V/V}$$

as we need overall gain as 100 V/V , so at least three such amplifiers are cascaded,

Now if each of 3-stages has closed loop gain K , then its 3-dB frequency will be $\frac{40}{K} \text{ MHz}$.

So for each stage the closed loop gain is

$$A = \frac{K}{\sqrt{1 + \left(\frac{f}{f_{3d}}\right)^2}}$$

overall gain is 100 so,

$$100 = \left| \frac{K}{\sqrt{1 + \left(\frac{K}{8}\right)^2}} \right|^3$$

by solving $K = 5.7$

So for each cascading stage,

$$f_{3 \text{ dB}} = \frac{40}{5.7}$$

$$f_{3 \text{ dB}} = 7 \text{ MHz}$$

So for overall amplifier total f_T is

$$\left| \frac{5.7}{\sqrt{1 + \left(\frac{f_T}{7}\right)^2}} \right|^3 = \frac{(5.7)^3}{\sqrt{2}}$$

$$f_T = 3.6 \text{ MHz}$$

- 1.9 A particular inverting amplifier with nominal gain of -100 V/V uses an imperfect Op-amp in conjunction with $100 \text{ k}\Omega$ and $10 \text{ M}\Omega$ resistors. The output voltage is found to be $+9.31 \text{ V}$ when measured with the input open and 9.09 V with the input grounded.

- What is the bias current of this amplifier? In what direction does it flow?
- Estimate the value of the input offset voltage.
- A $10 \text{ M}\Omega$ resistor is connected between the positive input terminal and ground with the input left floating (disconnected), the output dc voltage is measured to be -0.8 V , estimate the input offset current. (15 Marks)

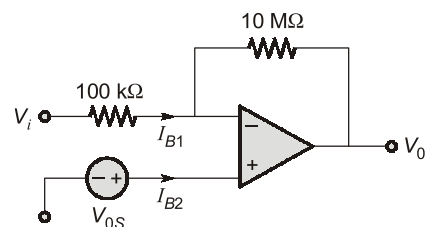
Solution:

(a) $\therefore I_B = \frac{(I_{B1} + I_{B2})}{2}$

When input is open :

$$V_0 = V_{0s} + 100KI_{B1}$$

$$9.31 = V_{0s} + 10000I_{B1}$$



...(i)

When input connected to ground:

$$V_0 = V_{0s} + R_2 \left(I_{B1} + \frac{V_{0s}}{R_1} \right)$$

$$V_0 = V_{0s} \left(1 + \frac{R_2}{R_1} \right) + R_2 I_{B1}$$

$$9.09 = V_{0s}(101) + 10000 I_{B1} \quad \dots(ii)$$

From (i) and (ii), [(1) – (2)]

$$100 V_{0s} = -0.22$$

$$V_{0s} = -2.2 \text{ mV}$$

and

$$I_{B1} = 930 \text{ nA}$$

So,

$$I_B \approx I_{B1} = 930 \text{ nA}$$

(b) input offset voltage, $V_{0s} = -2.2 \text{ mV}$

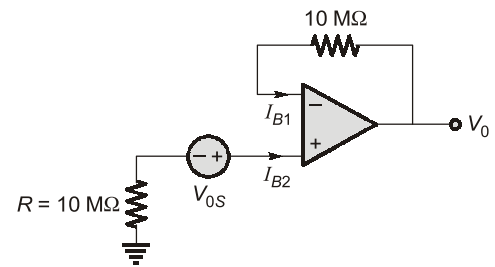
(c) Here V_{0s} can be neglected as magnitude of R is very large

$$\therefore V_{0s} \ll R I_B$$

$$V_0 = I_{0s} \times R_2$$

$$Z_{0s} = \frac{-0.8}{10M}$$

$$I_{0s} = -80 \text{ nA}$$



2. Diodes

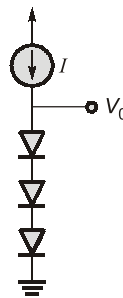
Level-1

- 2.1 The circuit in the figure utilizes three identical diodes having $\eta = 1$ and $I_s = 10^{-14} \text{ A}$. Find the value of the current I required to obtain an output voltage $V_0 = 2 \text{ V}$. If a current of 1 mA is drawn away from the output terminals by a load, what is the change in output voltage? (8 Marks)

Solution:

As each diode is identical. So the voltage across each diode is $\frac{V_0}{3}$.

$$\begin{aligned} \text{and diode current, } I &= I_s e^{\frac{V_0/3}{4V_T}} = 10^{-14} e^{\frac{2/3}{0.025}} \\ &= 3.81 \text{ mA} \end{aligned}$$

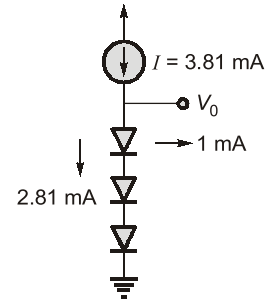


Now, let's say now the changed voltage across each diode is ΔV .

$$\frac{I_2}{I_1} = e^{\frac{(V_2 - V_1)/3}{0.025}}$$

$$\frac{2.81}{3.81} = e^{\frac{(V_2 - 2)/3}{0.025}}$$

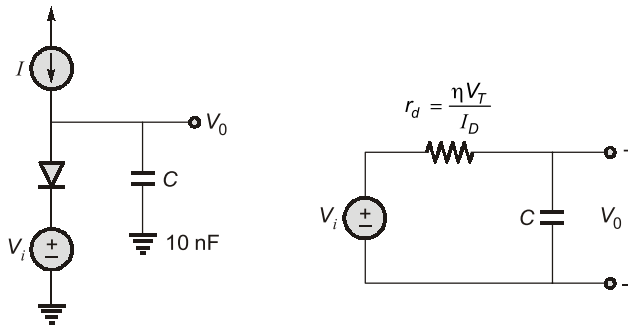
$$\Delta V = V_2 - 2 = -22.8 \text{ mV}$$



- 2.2 In the circuit shown in figure, I is a dc current and V_i is the sinusoidal signal with small amplitude (less than 10 mV) and a frequency of 100 kHz. Representing the diode by its small signal resistance r_d which is a function of I , sketch the circuit for determining the sinusoidal output voltage V_0 and thus find the phase shift between V_i and V_0 . Find the value of I that will provide a phase shift of -45° and find the range of phase shift achieved as I is varied over the range of 0.1 to 10 times this value ($\eta = 1$). (10 Marks)

Solution:

To get small signal circuit we open the current source and then we draw the circuit as:



$$\frac{V_0}{V_i} = \frac{1/SC}{\frac{1}{SC} + r_d} = \frac{1}{1 + SCr_d}$$

$$\begin{aligned} \text{Phase shift} &= -\tan^{-1} \left[\frac{\omega Cr_d}{1} \right] \\ &= -\tan^{-1} \left(2\pi \times 10^5 \times 10 \times 10^{-9} \times \frac{0.025}{I} \right) \end{aligned}$$

as we know that the phase shift is -45°

$$\text{So } -45^\circ = -\tan^{-1} \left(2\pi \times 10^5 \times 10 \times 10^{-9} \times \frac{0.025}{I} \right)$$

$$2\pi \times 10^3 \times \frac{0.025}{I} = 1$$

$$I = 157 \mu\text{A}$$

Range of phase shift for $I = 15.7 \mu\text{A}$ to $1570 \mu\text{A}$ is

For

$$I = 15.7 \mu\text{A}$$

$\Rightarrow$

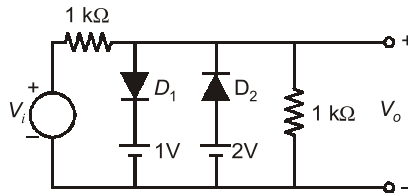
$$\phi_1 = -\tan^{-1} \left[2\pi \times 10^{-3} \times \frac{0.025}{15.7 \mu\text{A}} \right] = -84.3^\circ$$

$$I = 1570 \mu\text{A}$$

$$\Rightarrow \phi_2 = -\tan^{-1} \left[2\pi \times 10^{-3} \times \frac{0.025}{15.7 \mu\text{A}} \right] = -5.71$$

So range is -84.3° to -5.71° .

- 2.3 (i) Draw the transfer characteristics of the circuit of figure, assuming both D_1 and D_2 to be ideal
(ii) How would the characteristics change if D_2 is ideal, but D_1 is no-ideal and has a forward resistance of 10Ω and a reverse of infinity.



(5 Marks)

Solution:

- (i) Given that both the diodes are ideal, so when the diode is forward bias then it will act as short circuit and when the diode is reverse bias then it will act as open circuit.

When V_o is between 1 V to 2 V.

$$1 \text{ V} \leq V_o \leq 2 \text{ V}$$

in this case both the diodes D_1 and D_2 are forward bias.

1 V and 2 V can not be in parallel and its violation of KVL.

So, this circuit does not exist.

- (ii) $V_o \leq 2 \text{ V}$ (D_2 F.B. and D_1 F.B.)

Apply KCL

$$\begin{aligned} I + I_1 &= I_2 + I_3 \\ \frac{V_i - 2}{1\text{k}} + I_1 &= \frac{2 - 1}{10} + \frac{2 - 0}{1\text{k}} \\ I_1 &= \frac{104 - V_i}{1000} \\ I_1 &\geq 0 \end{aligned}$$

$$\frac{104 - V_i}{1000} \geq 0$$

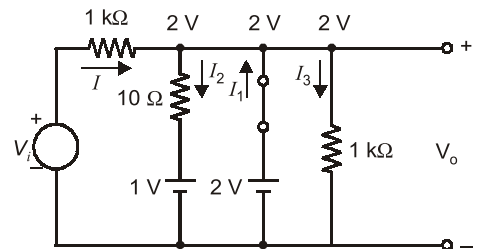
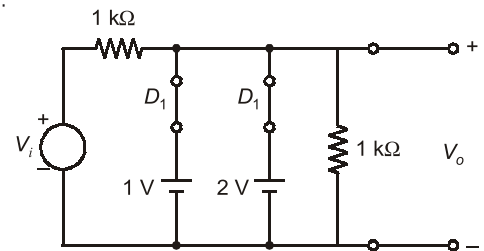
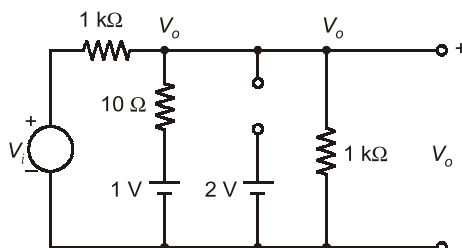
$$104 - V_i \geq 0$$

$$V_i \leq 104 \text{ V} \Rightarrow V_o = 2 \text{ V}$$

Case 2: $V_i \geq 104 \text{ V}$, So, $V_o \geq 2 \text{ V}$

Diode D_1 is forward bias.

Diode D_2 is reverse bias.



Apply KCL

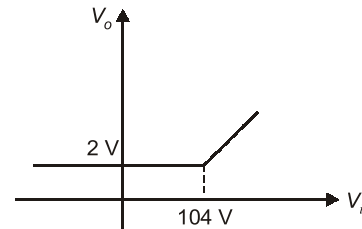
$$\frac{V_o - V_i}{1k} + \frac{V_o - 1}{10} + \frac{V_o - 0}{1k} = 0$$

$$\frac{V_o - V_i + 100 V_o - 100 + V_o}{1k} = 0$$

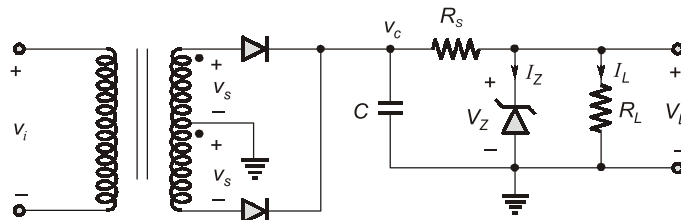
$$102 V_o - V_i - 100 = 0$$

$$102 V_o = V_i + 100$$

$$V_o = \frac{V_i + 100}{102}$$



2.4 Consider the circuit shown in the figure below:



The secondary voltage is given by $v_s = 24 \sin \omega t$ V. The Zener diode has parameters $V_Z = 15$ V at $I_Z = 20$ mA and $r_z = 10 \Omega$. Assume that all the diodes have a forward voltage drop of $V_f = 0$. The value of capacitance C is designed in such a way that the peak-to-peak ripple voltage is no larger than 1 V. Determine the maximum value of R_s such that load current can vary over the range $20 \text{ mA} \leq I_L \leq 180 \text{ mA}$ with $I_{Z(\min)} = 20 \text{ mA}$. Also find the minimum value of C required when the line frequency is 50 Hz.

(12 Marks)

Solution:

It is given that the maximum peak-to-peak ripple voltage is 1 V.

So, $V_{c(\min)} = 24 - 1 = 23$ V

$$R_s = \frac{V_{c(\min)} - V_Z}{I_{Z(\min)} + I_{L(\max)}} = \frac{23 - 15}{20 + 180} \text{ k}\Omega = 40 \Omega$$

For a full wave rectifier with capacitive filter,

$$V_r = \frac{V_P}{2fRC} \leq 1 \text{ V}$$

$$C \geq \frac{V_P}{2fR}$$

$V_P = 24$ V, $f = 50$ Hz and $R_{\max} \approx R_{s(\max)} + r_z = 50 \Omega$.

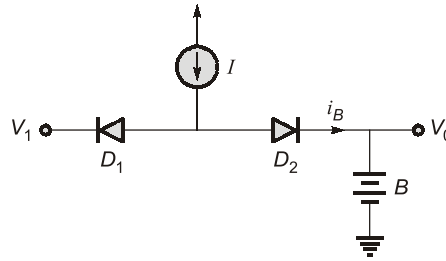
$$\text{So, } C_{\min} = \frac{24}{2 \times 50 \times 50} \text{ F} = 4.8 \text{ mF}$$

Level-2

2.5 The circuit shown in figure is a model for a battery charger. Here V_i is a 10 V peak sine wave, D_1 and D_2 are ideal diodes, I is a 100 mA current source and B is a 4.5 V battery.

- Sketch and level the waveform of the battery current i_B .
- What is the peak value?

- (c) What is its average value?
- (d) If the peak value of V_I is reduced by 10%, what do the peak and average values of i_B become?
- (20 Marks)



Solution:

- (a) By the figure we can observe that when $V_I < 4.5$ volt, D_1 conducts and D_2 is cutoff so $i_B = 0$. For $V_I > 4.5$ volt, D_2 conducts and D_1 is cutoff and all the current flows through the battery.

$$\text{conduction angle} = \pi - 2\theta$$

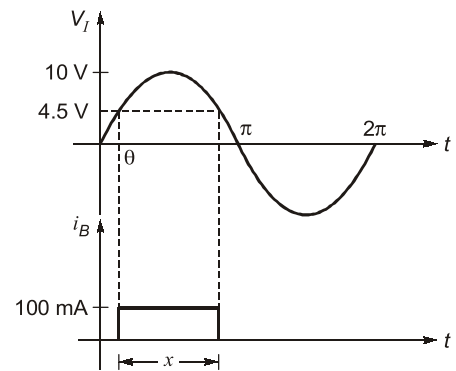
$$\therefore 10 \sin \theta = 4.5$$

$$\theta = \sin^{-1}\left(\frac{4.5}{10}\right)$$

- (b) Fraction of cycle for that $i_B = 100$ mA is

$$x = \frac{\pi - 2\theta}{2\pi} = \frac{\pi - 2\sin^{-1}\left(\frac{4.5}{10}\right)}{2\pi}$$

$$= 0.351$$



- (c)
$$i_{B \text{ avg}} = \frac{1}{T} \int i_B dt = \frac{1}{T} [100(0.35T)] = 35 \text{ mA}$$

- (d) If V_I is reduced by 10% the peak value of the i_B remains same.

$$\text{So } i_{B \text{ peak}} = 100 \text{ mA}$$

But the fraction of the cycle for conduction changes.

$$x = \frac{\pi - 2\theta}{2\pi} = \frac{\pi - 2\sin^{-1}\left(\frac{4.5}{9}\right)}{2\pi} = \frac{1}{3}$$

$$\text{Thus, } i_{B \text{ avg}} = \frac{1}{T} \left[100 \cdot \frac{T}{3} \right] = 33.3 \text{ mA}$$

- 2.6 In a particular circuit application, ten 20 mA diodes (a - 20 mA diode is a diode that provides a 0.7 V drop when the current through it is 20 mA) connected in parallel operate at a total current of 0.1 A. For the diodes closely matched, with $\eta = 1$.

- (a) What current flows in each?
- (b) What is the corresponding small signal resistance of each diode and of the combination?
- (c) Compare this with the incremental resistance of a single diode has a series resistance of 0.2Ω associated with the wire bonds to the junction.
- (d) What is the equivalent resistance of the 10 parallel-connected diodes?
- (e) What connection resistance would be single diode need in order to be totally equivalent?

(15 Marks)